1. Overview

TM1727 is a 4*40 LCD display drive control special circuit, which can display up to 160 segments. MCU two-wire digital interface, data latch, LCD driver and other circuits are integrated inside. Support 1/3base, 1/2base, line flip, frame flip, and 3v/5v LCD screen. All settings transmit data through the 2-wire serial interface. It is mainly used in segment code LCD display product driver.

2. Characteristic description

- Low power CMOS process
- 40x4 point LCD driver
- 1/2 or 1/3lcd drive bias optional
- support two driving waveforms of frame and line, and choose frame with lower power consumption
- Display brightness free setting
- Serial interface (SDA, SCL)
- Oscillation mode: built in RC oscillation
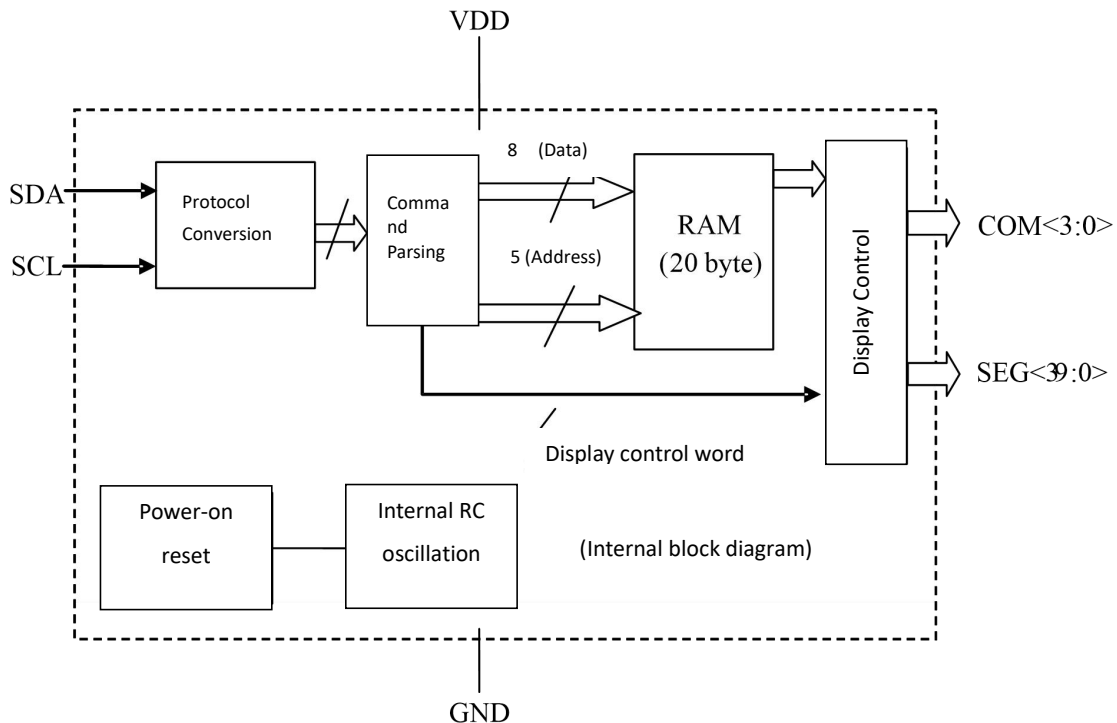- Packaging form: ssop48, lqfp48

3：   Principle block diagram

Figure 1: schematic block diagram

V1.2

4： Pin arrangement and pin description
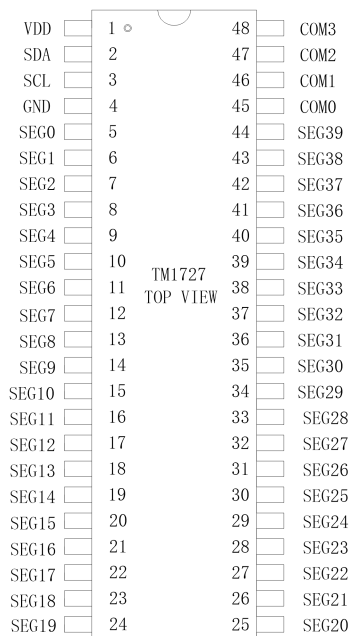
4.1 pin arrangement

```
         VDD  ┌─ 1  ○         48 ─┐  COM3
         SDA  ┌─ 2              47 ─┐  COM2
         SCL  ┌─ 3              46 ─┐  COM1
         GND  ┌─ 4              45 ─┐  COM0
        SEG0  ┌─ 5              44 ─┐  SEG39
        SEG1  ┌─ 6              43 ─┐  SEG38
        SEG2  ┌─ 7              42 ─┐  SEG37
        SEG3  ┌─ 8              41 ─┐  SEG36
        SEG4  ┌─ 9              40 ─┐  SEG35
        SEG5  ┌─ 10             39 ─┐  SEG34
        SEG6  ┌─ 11   TM1727    38 ─┐  SEG33
        SEG7  ┌─ 12  TOP VIEW   37 ─┐  SEG32
        SEG8  ┌─ 13             36 ─┐  SEG31
        SEG9  ┌─ 14             35 ─┐  SEG30
       SEG10  ┌─ 15             34 ─┐  SEG29
       SEG11  ┌─ 16             33 ─┐  SEG28
       SEG12  ┌─ 17             32 ─┐  SEG27
       SEG13  ┌─ 18             31 ─┐  SEG26
       SEG14  ┌─ 19             30 ─┐  SEG25
       SEG15  ┌─ 20             29 ─┐  SEG24
       SEG16  ┌─ 21             28 ─┐  SEG23
       SEG17  ┌─ 22             27 ─┐  SEG22
       SEG18  ┌─ 23             26 ─┐  SEG21
       SEG19  ┌─ 24             25 ─┐  SEG20
```

Figure 2: TM1727-ssop48 pin arrangement

```
              COM3 COM2 COM1 COM0 SEG39 SEG38 SEG37 SEG36 SEG35 SEG34 SEG33 SEG32
               48   47   46   45   44    43    42    41    40    39    38    37

        VDD ─┤ 1  ○                                    36 ├─ SEG31
        SDA ─┤ 2                                        35 ├─ SEG30
        SCL ─┤ 3                                        34 ├─ SEG29
        GND ─┤ 4                                        33 ├─ SEG28
       SEG0 ─┤ 5                                        32 ├─ SEG27
       SEG1 ─┤ 6            TM1727                       31 ├─ SEG26
       SEG2 ─┤ 7                                         30 ├─ SEG25
       SEG3 ─┤ 8           TOP  VIEW                     29 ├─ SEG24
       SEG4 ─┤ 9                                         28 ├─ SEG23
       SEG5 ─┤ 10                                        27 ├─ SEG22
       SEG6 ─┤ 11                                        26 ├─ SEG21
       SEG7 ─┤ 12                                        25 ├─ SEG20

               13   14   15   16   17   18   19   20   21   22   23   24
             SEG8 SEG9 SEG10 SEG11 SEG12 SEG13 SEG14 SEG15 SEG16 SEG17 SEG18 SEG19
```

Figure 3: TM1727-lqfp48 pin arrangement

4.2: pin description

Pin serial number	Pin name	Function description
2	SDA	2-wire serial communication data input
3	SCL	2-wire serial communication clock input
45-48	COM0-COM3	Bit drive
5-44	SEG0-SEG39	Segment drive
4	GND	land
1	VDD	Power Supply

5：   Display RAM distribution

This register stores the data sent from external devices to TM1727 through the serial interface. The address is 20 byte units from 00-13h, which corresponds to the LCD lamp connected to the chip SEG and com pins respectively. The address allocation is as follows:

	B0	B1	B2	B3	B4	B5	B6	**B7**
RAM address	COM0	COM1	COM2	COM3	COM0	COM1	COM2	COM3
00H		SEG0				SEG1		
01H		SEG2				SEG3		
02H		SEG4				SEG5		
03H		SEG6				SEG7		
04H		SEG8				SEG9		
05H		SEG10				SEG11		
06H		SEG12				SEG13		
07H		SEG14				SEG15		
08H		SEG16				SEG17		
09H		SEG18				SEG19		
0AH		SEG20				SEG21		
0BH		SEG22				SEG23		
0CH		SEG24				SEG25		
0DH		SEG26				SEG27		
0EH		SEG28				SEG29		
0FH		SEG30				SEG31		
10H		SEG32				SEG33		
11H		SEG34				SEG35		
12H		SEG36				SEG37		
13H		SEG38				SEG39		

Table 1: RAM address allocation

6： Communication protocol

TM1727 adopts 2-wire serial transmission protocol for communication.

1: Start / stop signal

Start signal: keep SCL at "1" level, and SDA jumps "0" from "1", which is considered as the start signal, such as (Figure 3) section a;

End signal: keep SCL at "1" level, and SDA jumps from "0" to "1", which is considered as the end signal, such as (Figure 3) section E;

2: ACK signal

If the communication is normal this time, the chip will actively pull the SDA down after the eighth clock falling edge of serial communication. Until the rising edge of SCL is detected, SDA is released to the input state (for the chip), as shown in segment D (Figure 3).

3: Write "1" and "0".

Write "1": keep SDA at "1" level, and when SCL jumps from "0" to "1", and then from "1" to "0", it is considered to be writing "1", as shown in paragraph B (Figure 3).

Write "0": keep SDA at "0" level, and SCL jumps from "0" to "1", and then from "1" to "0", it is considered to be writing "0", as shown in (Figure 3) segment C.
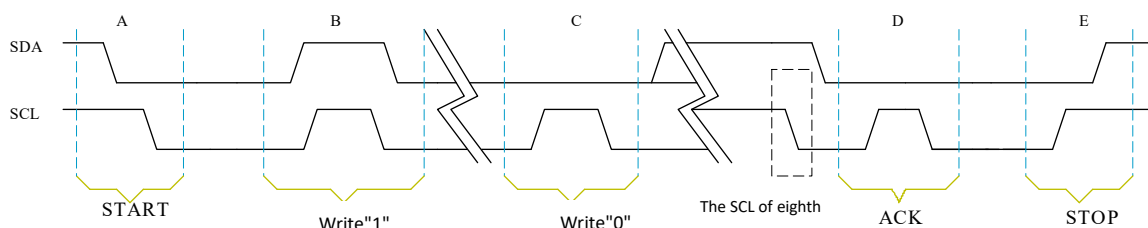
Figure 3

4: One byte data transmission format

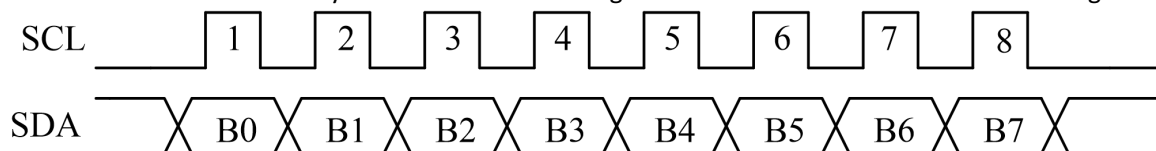The transmission format of a byte of data is shown in Figure 4. LSB is in front of MSB when sending data.

Figure 4

5: Display control commands

B7	B6	B5	B4	B3	B2	B1	B0
0	TESE	STANDBY	LF	BASE	PWM2	PWM1	PWM0

Test: =0, normal working mode= 1 test mode. In the test mode, the clock of the chip is switched to SCL. When it is switched from the normal working mode to the test mode, the display cycle of the chip is reset and a new scanning cycle is restarted.

Standby: =0, standby mode= 1. Normal working mode. In standby mode, both SEG and com are pulled up, and the internal oscillator stops working.

Lf:=0, line mode= 1frame mode.

BASE： =0，1/3BASE；= 1，1/2BASE

Pwm: the display brightness adjustment can only be effective for the screen driven by 3V voltage. If you are not satisfied with the display brightness by using 5V LCD, you can adjust the power supply voltage of IC (see Table 2).

V1.2

PWM<2:0>	Driving voltage (V)	explain
111	5.0	Drive 5V screen
110	3.3	Drive 3V screen
101	3.2	
100	3.1	
011	3.0	
010	2.9	
001	2.8	
000	2.7	

Table 2: driving voltage corresponding to PWM setting

6: Data command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	0	Starting address				

The set address is the starting address. The address range is 00h-13h

7: Send display control command format

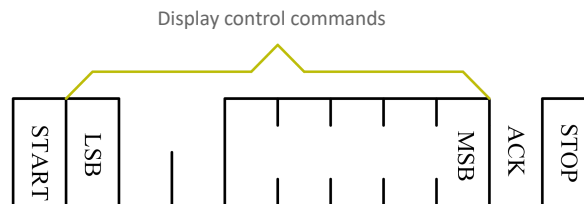| Start signal	Display control commands	ack	End signal

Display control commands

Figure 5

LSB is in front and MSB is in the back when sending data.

8: Send display data format

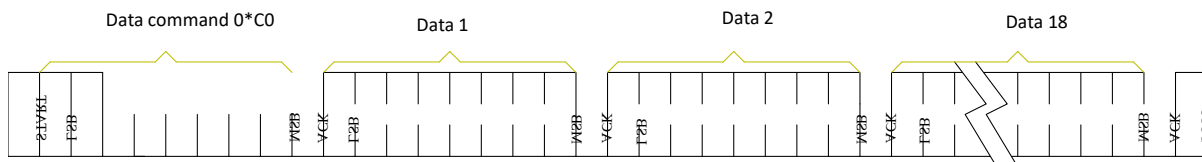| Start signal	Data command	ack	Data 1	ack	Data 2	ack	....	Data n (end)	ack	End signal

Data command 0*C0   Data 1   Data 2   Data 18

Figure 6

Data transmission starts with "start" and ends with "stop". LSB is in front and MSB is in the back when sending data. The sending of display data only supports the automatic address plus one method, that is, every time 1byte data is received, the address will be automatically plus one, and there is no need to reset the address. TM1727 internal RAM has 32 byte addresses (00-1fh), and the actual display RAM is only 00h-13h (20byte). When the address is 13h, continue to send data, and add one to the address. Since the display RAM is only 20byte, it does not affect the chip display RAM. When the address is 1fh, continue to send data, and the address plus one equals 00h, which will rewrite the content of 00h unit.
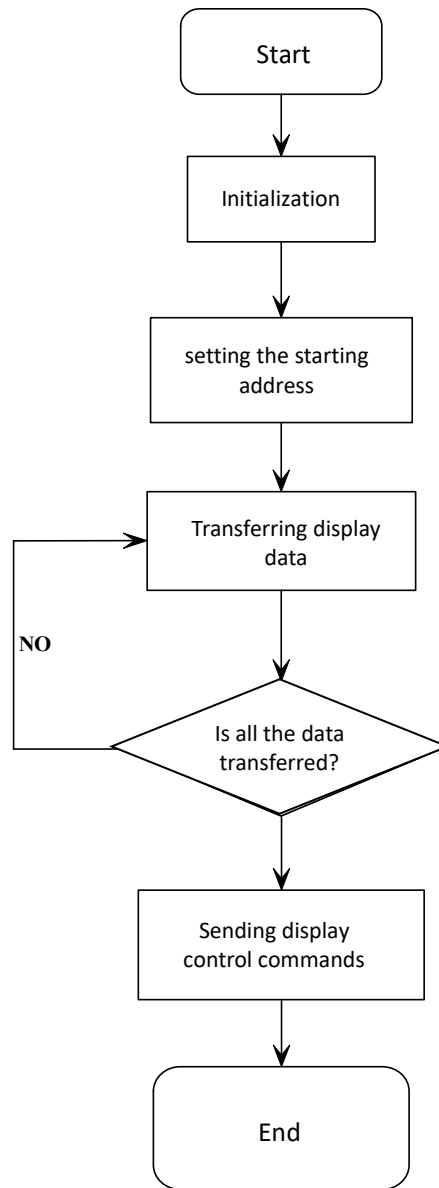
© Titan Micro Electronics www.titanmec.com

V1.2

7： Procedure flow chart:

```
                    ┌─────────────┐
                    │    Start    │
                    └──────┬──────┘
                           │
                           ▼
                    ┌─────────────┐
                    │ Initialization │
                    └──────┬──────┘
                           │
                           ▼
                  ┌───────────────┐
                  │ setting the starting │
                  │    address    │
                  └───────┬───────┘
                          │
                          ▼
       ┌──────────┌───────────────┐
       │          │ Transferring display │
       │          │     data      │
       │          └───────┬───────┘
  NO   │                  │
       │                  ▼
       │          ◇───────────────◇
       └──────────  Is all the data
                    transferred?
                  ◇───────────────◇
                          │
                          ▼
                  ┌───────────────┐
                  │ Sending display │
                  │ control commands │
                  └───────┬───────┘
                          │
                          ▼
                    ┌─────────────┐
                    │     End     │
                    └─────────────┘
```

Figure 7: flow chart

V1.2

8： Driving waveform

Taking seg0-com3 as an example, the driving waveform is given
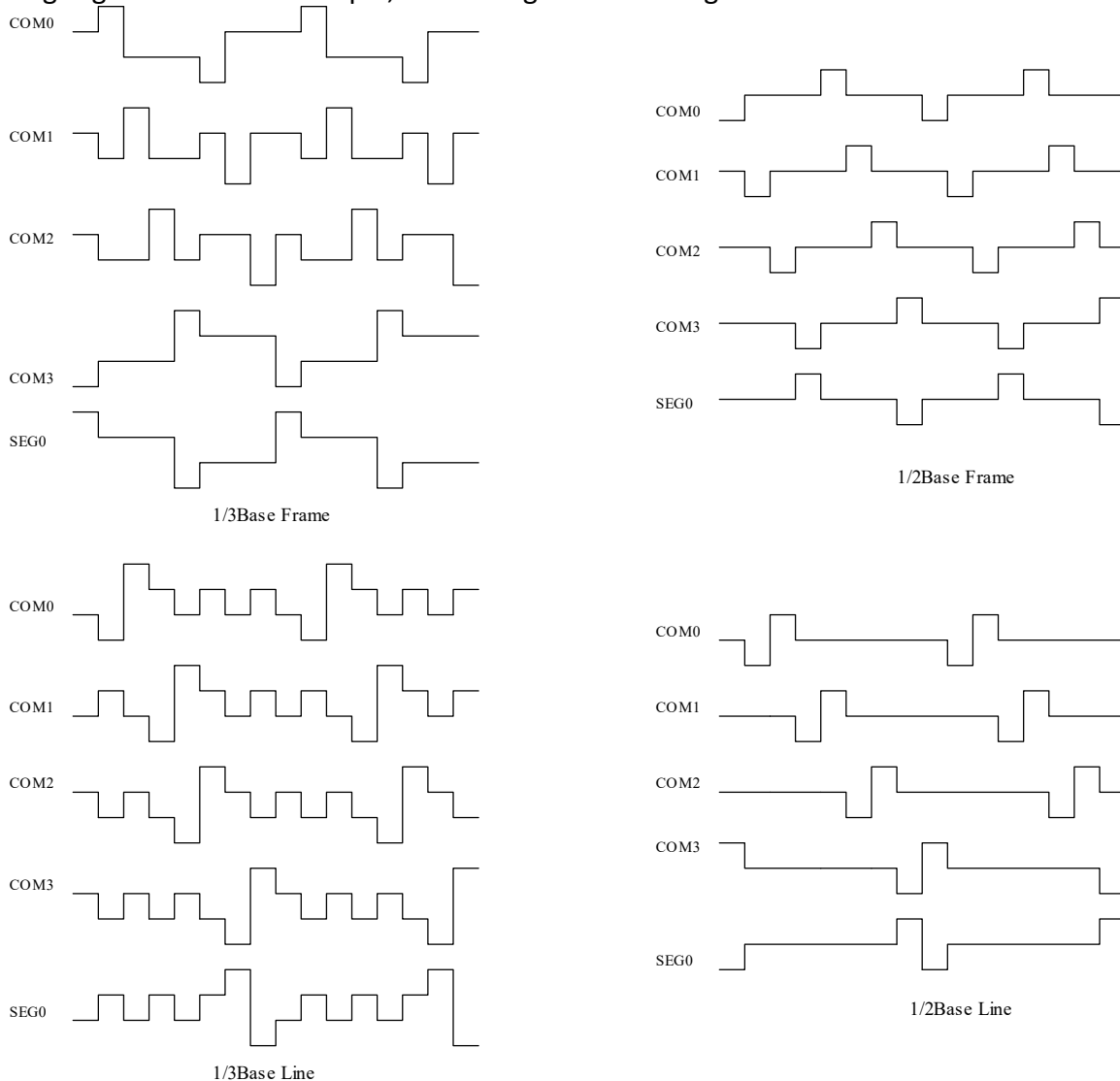

1/3Base Frame

1/2Base Frame

1/3Base Line

1/2Base Line

Figure 8 driving waveform

9： Electrical parameters:

1: Limit parameter (TA = 25 ℃, VSS = 0 V)

parameter	Symbol	Range	Unit
Logic supply voltage	VDD	-0.5 ～+6.0	V
Logic input voltage	VI1	-0.5 ～ VDD + 0.5	V
working temperature	Topt	-40 ～ +105	℃
Storage temperature	Tstg	-65 ～+150	℃

2: Electrical characteristics in normal working range (TA = -20 ~ +70 ℃, VDD = 5V, VSS = 0 V

parameter	Symbol	minimum	typical	maximum	Unit	Test conditions
Logic supply voltage	VDD	-	5	-	V	-
Normal operating current	IDD	-	10	-	uA	
Standby current	IDD0	-	-	1	uA	
High level input voltage	VIH	0.65 VDD	-	VDD	V	
Low level input voltage	VIL	0	-	0.4 VDD	V	-
LCD com output current	IOH1	-120	-150	-	uA	COM0~COM3 Vo=4.5V
LCD com input current	IOL1	80	100	-	uA	COM0~COM3 Vo=0.5V
LCD SEG output current	IOH2	-80	-150	-	uA	SEF0-SEG35 Vo=4.5V
LCD SEG input current	IOL2	80	100	-	uA	SEF0-SEG35 Vo=0.5V

3: Switching characteristics (TA = -20 ~ +70 ℃, VDD = 5 V)

parameter	Symbol	minimum	typical	maximum	Unit	Test conditions
oscillation frequency	fosc	-	95	-	KHz	
Maximum clock frequency	fmax	12	-	-	KHz	Duty cycle 50%

4: Timing characteristics (TA = -20 ~ +70 ℃, VDD = 5 V)

parameter	Symbol	minimum	typical	maximum	Unit	Test conditions
Clock pulse width	PWCLK	400	-	-	ns	-
Data establishment time	tSETUP	100	-	-	ns	-
Data retention time	tHOLD	100	-	-	ns	

5: Time sequence waveform:

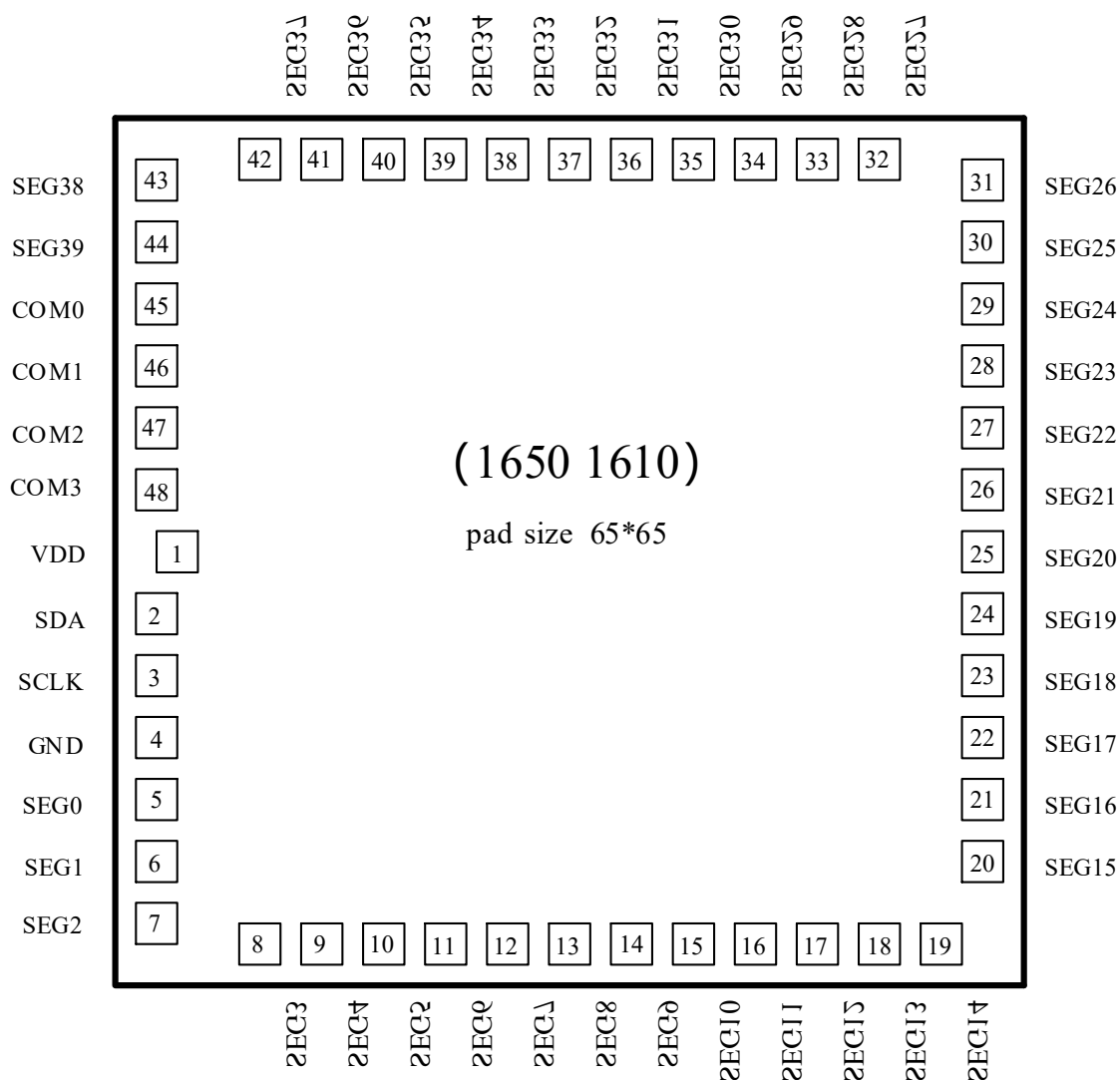
Figure 9: timing waveform

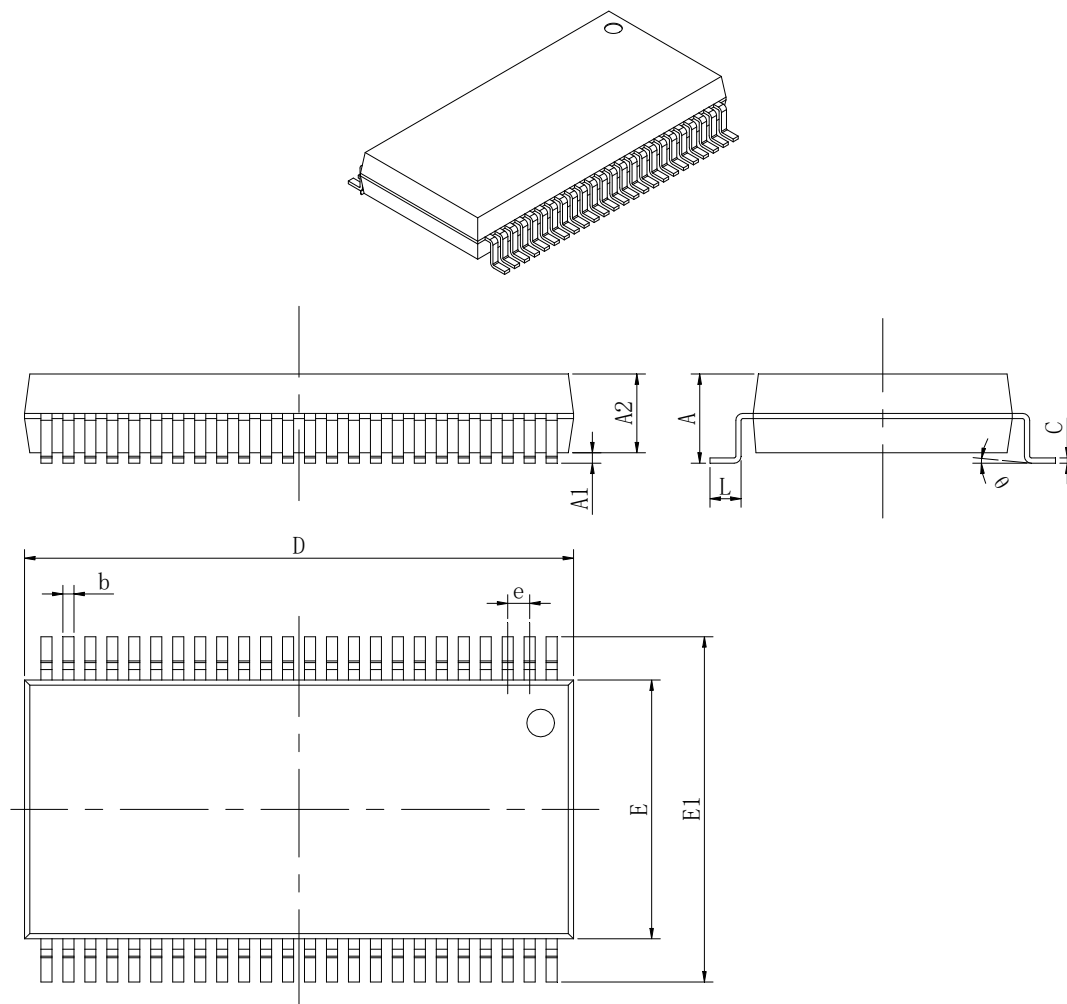# 10、 Binding diagram:

Uint:um

Figure 10

Pin coordinates:

Unit:um

Pad No.	X	Y	Pad No.	X	Y
1	149	811	25	1541	820
2	113	696	26	1541	930
3	113	586	27	1541	1040
4	113	476	28	1541	1150
5	113	366	29	1541	1260
6	113	256	30	1541	1370
7	113	146	31	1541	1480
8	291	110	32	1383	1500
9	401	110	33	1273	1500
10	511	110	34	1163	1500
11	621	110	35	1053	1500
12	731	110	36	943	1500
13	841	110	37	833	1500
14	951	110	38	723	1500
15	1061	110	39	613	1500
16	1171	110	40	503	1500
17	1281	110	41	393	1500
18	1391	110	42	283	1500
19	1500	110	43	113	1473
20	1541	270	44	113	1363
21	1541	380	45	113	1253
22	1541	490	46	113	1143
23	1541	600	47	113	1033
24	1541	710	48	113	923

11： Encapsulation

Ssop48 package diagram:

Symbol	Unit: mm		Unit: Inch	
	minimum	maximum	minimum	maximum
A	2.41	2.78	0.095	0.109
A1	0.20	0.40	0.008	0.016
A2	2.18	2.38	0.086	0.094
b	0.20	0.35	0.008	0.014
c	0.20	0.40	0.008	0.016
D	15.77	15.97	0.621	0.629
E	7.39	7.59	0.291	0.299
E1	10.01	10.61	0.394	0.418
e	0.635(BSC)		0.025(BSC)	
L	0.61	0.91	0.024	0.036
θ	0°	8°	0°	8°

V1.2

Lqfp48 package diagram:

Symbol	Unit: mm		Unit: Inch	
	minimum	maximum	minimum	maximum
A		1.600		0.063
A1	0.050	0.150	0.002	0.006
A2	1.350	1.450	0.053	0.057
b	0.190	0.260	0.007	0.010
c	0.090	0.200	0.004	0.008
D	6.900	7.100	0.272	0.280
D1	8.850	9.150	0.348	0.360
E	6.900	7.100	0.272	0.280
E1	8.850	9.150	0.348	0.360
e	0.500(BSC)		0.020(BSC)	
L	0.450	0.750	0.018	0.030
θ	1°	7°	1°	7°

All specs and applications shown above subject to change without prior notice by Titanmec.